# **Instruction Cycle**

#### **INSTRUCTION FETCH**

 $MAR \leftarrow PC$   $MDR \leftarrow memory[MAR]$   $IR \leftarrow MDR$   $PC \leftarrow PC + 1$ 

#### **DECODE**

Opcode in IR[15:12] interpreted by Control Unit Operand fields in IR[11:0] interpreted

## **EVALUATE ADDRESS (Data Move Instructions)**

Calculate memory address from instruction

#### **OPERAND FETCH (Operate & Data Move Instructions)**

Output source registers to ALU inputs
Read data from memory into MDR
Load
Transfer data from source register to MDR
Store

### **EXECUTE** (Operate & Control Instructions)

Required ALU operation is performed Operate PC overwritten with branch address Control

### **STORE RESULT (Operate & Data Move Instructions)**

Store ALU output into destination register Operate
Write data from MDR into memory Store
Transfer data from MDR to destination Register Load